UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/722,636 | 11/25/2003 | William C. Plants | ACT-280COA | 7317 |

28661 7590 01/12/2005

SIERRA PATENT GROUP, LTD.
P O BOX 6149
STATELINE, NV 89449

| EXAMINER | |
|---|---|
| CHANG, ERIC | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/722,636 | PLANTS ET AL. | |
| | Examiner | Art Unit | |
| | Eric Chang | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-12 are pending.

### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,718,477 to Plants, et al. Although the conflicting claims are not identical, they are not patentably distinct from each other because they both claim an apparatus and method for a delay lock loop comprising the same elements sharing the same relationships to each other.

4. As to claim 1, Plants discloses the limitations of the claim [col. 9, lines 2-30], including a control logic circuit having an input programmably coupled to an output of a phase detector [col. 9, lines 19-20] but does not teach that the control logic circuit has a plurality of inputs and a plurality of outputs. At the time that the invention was made, it would have been obvious to a

person of ordinary skill in the art to employ a plurality of inputs and a plurality of outputs for the coupling of the control logic circuit. One of ordinary skill in the art would have been motivated to do so that a multi-bit control signal can be used to program the programmable delay line, which would inherently be necessary unless the programmable delay line comprises a single binary setting. Furthermore, Plants discloses that it would be obvious to one of ordinary skill in the art to use the output of a delay lock loop to synchronize the clock of a flip-flop [col. 1, lines 11-21], substantially as claimed.

5. As to claim 2, Plants discloses a primary and secondary delay line, as well as a pulse shaper [col. 9, lines 31-47].

6. As to claim 3, Plants discloses the reference clock is an external clock [col. 9, lines 3-5].

7. As to claim 4, Plants discloses the reference clock is an internal clock [col. 9, lines 3-5].

8. As to claims 5-6, Plants discloses programmable delay lines controlled by a plurality of control bits [col. 9, lines 31-45]. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to employ delay quanta in the construction of the programmable delay lines. One of ordinary skill in the art would have been motivated to do so that the delay imparted by the programmable delay line could be set to a discrete amount based on the plurality of control bits.

9. As to claim 7, Plants discloses the limitations of the claim [col. 9, lines 48-49 and col. 10, lines 1-30], including a control logic circuit having an input programmably coupled to an output of a phase detector [col. 9, lines 19-20] but does not teach that the control logic circuit has a plurality of inputs and a plurality of outputs. At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ a plurality of inputs and a plurality of outputs for the coupling of the control logic circuit. One of ordinary skill in the art would have been motivated to do so that a multi-bit control signal can be used to program the programmable delay line, which would inherently be necessary unless the programmable delay line comprises a single binary setting.

10. As to claim 8, Plants discloses a primary and secondary delay line, as well as a pulse shaper [col. 10, lines 31-47].

11. As to claim 9, Plants discloses the reference clock is an external clock [col. 10, lines 1-2].

12. As to claim 10, Plants discloses the reference clock is an internal clock [col. 10, lines 1-2].

13. As to claims 11 and 12, Plants discloses programmable delay lines controlled by a plurality of control bits [col. 10, lines 31-45]. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to employ delay quanta in the construction of the programmable delay lines. One of ordinary skill in the art would have been motivated to do

so that the delay imparted by the programmable delay line could be set to a discrete amount based on the plurality of control bits.

***Conclusion***

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 7, 2005
ec

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100